REMARKS

Claims 1, 4-12, and 14-16 are pending. No new matter has been added by way of this amendment. Reconsideration of the application is requested.

Claims 1, 4, 7, and 8 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,317,820 to *Shiell* et al., while claims 5, 6, 9-12, 14, 15, and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the same reference in view of U.S. Patent No. 5,761,470 to *Yoshida*. Reconsideration of these several rejections is respectfully requested.

Independent claims 1, 12, and 15 recite the limitation that the "decode unit [is] operable to control the first and second channels such that, when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel to implement one of those operations and the second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously." This limitation is also set forth in method claim 8, which recites the "instruction defines two independent operations, supplying one of the operations to the first processing channel and the other of the operations to the second processing channel whereby the operations are executed simultaneously."

Set forth on page 3, paragraph 11 of the Office Action is the statement that:

> On page 8, Applicant argues in essence:
>
> "The instruction format and decode unit are configured such that the claimed computer system can execute single operations or dual operations, each employing the resources of the computer differently, based on the identification bits within the instruction (see ID1 and ID2 in Figs. 2a and 2b). As a consequence, only one decode unit and one set of instructions bit per predetermined bit length is needed. This drastically simplifies the fetch and decode instruction semantics require[d] to achieve a given level of performance, while retaining the capability of selecting between levels of instruction parallelism. This novel feature of the invention is reflected[ed] in all of the independent claims and is not disclosed in any of the presently cited prior art documents."

> However, since the claims do not define how the "detection" occurs, any manner of detecting single vs. dual operation instructions will read upon the claims.

With respect to the foregoing, however, Applicant respectfully asserts that stating that the claims fail to define "how the detection occurs" is contradictory to the statement that the detection aspect is not recited in the claims (see text below with respect to bits contained within the instruction). Applicant wish to direct the Examiner's attention to dependent claim 5. This claim recites the limitation that "the decode unit is operable to make the detection based on the values of a designated set of identification bits at predetermined bit locations in the instruction." In view of the foregoing, Applicant respectfully asserts that the argument is not moot, based on the language set forth in dependent claim 5 which demonstrates how the "detection" occurs.

Set forth on page 5, paragraph 12 of the Office Action is the statement that:

> On pages 9, 10, and 11, Applicant argues in essence:
>
> "However, Sheill et al. fail to teach the limitations the "decode unit being operable to control the first and second channels such that, when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel to implement one of those operations and a second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously," and the "instruction defines two independent operations, supplying one of the operation of the first processing channel and the other one of the operations to the second processing channel whereby the operations are executed simultaneously," as set forth in amended independent claims 1, 12, and 15 and method claim 8, respectively. Here the decision of whether to implement parallel processing is based on the bits ID1 and ID2 that are contained within the instruction itself."
>
> However, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the decision of whether to implement parallel processing is based on the bits ID1 and ID2 that are contained within the instruction itself) are not recited in the rejected claims 1, 12, and 15. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

> Furthermore Shiell et al. has in fact taught "decode unit being operable to control the first and second channels such that, when the decode unit detects that the instruction defines two independent operations (column 2, lines 23-56, Second mode) it is operable to control the first channel to implement one of those operations (column 2, lines 23-56, A side operation) and a second channel to implement the other of those operations (column 2, lines 23-56, B side operation), whereby the first and second channels execute their respective independent operations simultaneously (column 2, lines 23-56)," and the "instruction defines two independent operations, supplying one of the operation of the first processing channel and the other one of the operations to the second processing channel whereby the operations are executed simultaneously (column 2, lines 23-56)".

In response to the foregoing statements, Applicant respectfully points out that the text of the *Shiell* et al. patent reference by the Examiner states:

> This invention is a very long instruction word ***data processor***... The ***data processor*** may be selectively operable in either a first or second mode (see col. 2, lines 23-27)....
>
> In the second mode the ***data processor*** can [process] two independent program instruction streams simultaneously. The ***data processors*** includes plural control registers, at least one control register having duplicated for the A side and the B side (see col. 2, lines 43-47)....
>
> The ***data processor*** may be changed from the first mode to the second mode and from the second mode to the first mode via instructions or the state of a control register (see col. 2, lines 53-55). (emphasis added)

As a result, Applicant respectfully wishes to point out that the claims include the limitation, "a decode unit for decoding instructions" and also recite "a data processing unit." The sections referenced by the Examiner state a data processor is selectively operable in either a first or second mode. Applicant is not claiming a data processor which is operable to control first and second channels, rather Applicant is claiming a decode unit which is operable to control the first and second channels. In the claimed invention, there is a data processor that includes a decode unit that functions as claimed, where the data processor also performs separate functions. This simply is not the case with the cited reference. As a result, Applicant respectfully asserts that the *Shiell* et al. patent simply fails to teach or suggest the configuration which is set forth and claimed.

As stated previously, the system disclosed in *Shiell* et al. is directed to supplying additional (duplicate) components so that the computer can support both a first mode of operation and a second mode of operation. In the first mode, the data processor executes a single instruction stream. In the second mode, the data processor executes two independent program instruction streams simultaneously. To do this, fetch/decode circuitry is divided into two parts 115A and 115B each serving a separate side (see for example col. 4, lines 35-44). In addition, fetch program counter and control units 110A and 110B are each used to fetch a half packet of instructions, (1/2 of a VLIW eight instruction packet) from program memory 105 (which is now dual ported), into respective Instruction Dispatch/Decode units 115A and 115B (see col. 4, line 66 thru col. 5, line 4). This permits the CPU to process two instruction streams (each corresponding to half of the VILW 8 instruction packet) simultaneously. However, Applicants respectfully wish to re-assert that *Sheill* et al. fail to teach the limitations the "decode unit being operable to control the first and second channels such that, when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel to implement one of those operations and the second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously," and the "instruction defines two independent operations, supplying one of the operations to the first processing channel and the other of the operations to the second processing channel whereby the operations are executed simultaneously," as set forth in amended independent claims 1, 12 and 15, and method claim 8, respectively. Here the decision of whether to implement parallel processing is based on the bits ID1 and ID2 that are contained within the instruction itself, as set forth in independent claims 5 and 9.

In the *Sheill* et al. patent, a data processor 200 includes a decoder unit 115. However, the instructions provided from the decoder do not indicate whether parallel processing should be used, i.e., no signalling from within the instruction is used in this system. Rather, *Sheill* et al. requires separate control units 110A and 110B to produce the instruction streaming as taught therein. It follows that there is simply no ability for a single fixed length instruction to be flexible as to whether it is a single or multiple operation. Furthermore, the decoder of this patent operates in a manner which is different than the operation of the decoder of the claimed invention. Hence, it is

In view of the foregoing remarks, this application should be in condition for allowance. Early passage of this case to issue is respectfully requested. However, if there are any questions regarding this Response, or the application in general, a telephone call to the undersigned would be appreciated since this would expedite the prosecution of the application for all concerned.

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Respectfully submitted,

By _____

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Request for Reconsideration (7 pages)